

Q1 cont.
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sequences affecting the instruction execution in an optimum manner includes means for transmitting and switching signals to said elements optically.

Claim 2, line 3, change "the" to --an--.

Cancel claim 5.

Q2
11. (Amended) In a computer including a memory for holding a sequence of instructions to be executed, logic for accessing the instructions in sequence, logic for determining for each instruction [the] a function to be performed and [the] an effective address thereof, and logic for executing each instruction, [the improved] a method of operation comprising the steps of:

- a) providing a plurality of individual elements on a common support substrate with each element optimized to perform certain logical sequences employed in executing instructions; and for each instruction,
- b) determining the function to be performed;
- c) determining [the] a class of each function;
- d) causing the instruction to be executed by those elements which perform the associated logical sequences affecting the instruction execution in an optimum manner by optically transmitting and switching signals to the elements.

Claim 12, line 4, change "the" to --an--.

Cancel claim 13.

Q3
19. (Amended) A computer comprising:

- a) a memory for holding a sequence of instructions to be executed;
- b) logic for accessing said instructions in sequence;
- c) logic for determining for each said instruction [the] a function to be performed and [the] an effective address thereof;
- d) a plurality of individual elements on a common support substrate optimized to perform certain logical sequences employed in executing said instructions; and,
- e) element selection logic means connected to said logic determining the function to be performed for each said instruction for determining [the] a class of each function and for causing the instruction to be executed by those said elements which perform those associated said logical sequences affecting the instruction execution in an optimum manner, said element selection logic means portion for causing the instruction to be executed by those said elements which perform those associated said logical sequences affecting the instruction execution in an optimum manner including means for transmitting and switching signals to said elements optically.

Claim 20, line 3, change "the" to --an--.

Cancel claim 23.

Add the following new claims:

Sub
C3
37. In a computer including a memory for holding a sequence of instructions to be executed, logic for accessing the instructions in sequence, logic for determining for each instruction a function to be performed and an effective address thereof, and logic for executing each instruction, the improvement wherein:

a) the logic for executing instructions comprises a plurality of individual elements on a common support substrate optimized to perform certain logical sequences employed in executing instructions; and additionally comprising,

b) element selection logic means connected to the logic determining the function to be performed for each instruction for determining a class of each function and for causing the instruction to be executed by those said elements which perform those associated said logical sequences affecting the instruction execution in an optimum manner, said element selection logic means including means for accepting dynamic inputs designating changes in an operating environment of the computer and means for changing the ones of said elements which execute each instruction as a function of said dynamic inputs whereby instruction execution is affected in an optimum manner for the present dynamic conditions.

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38. A computer comprising:

a) a memory for holding a sequence of instructions to be executed;
b) logic for accessing said instructions in sequence;
c) logic for determining for each said instruction a function to be performed and an effective address thereof;

d) a plurality of individual elements on a common support substrate optimized to perform certain logical sequences employed in executing said instructions; and,

e) element selection logic means connected to said logic determining the function to be performed for each said instruction for determining a class of each function and for causing the instruction to be executed by those said elements which perform those associated said logical sequences affecting the instruction execution in an optimum manner, said element selection logic means including means for accepting dynamic inputs designating changes in the operating environment of the computer and means for changing the ones of said elements which execute each instruction as a function of said dynamic inputs whereby instruction execution is affected in an optimum manner for the present dynamic conditions.